REMARKS

Claims 1–26 are pending in the present application.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 102 (Anticipation)

Claims 1–6, 8–9, 12–17 and 20–26 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,907,514 to *Mitsuishi*. This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-76 (8th ed. rev. 4 October 2005).

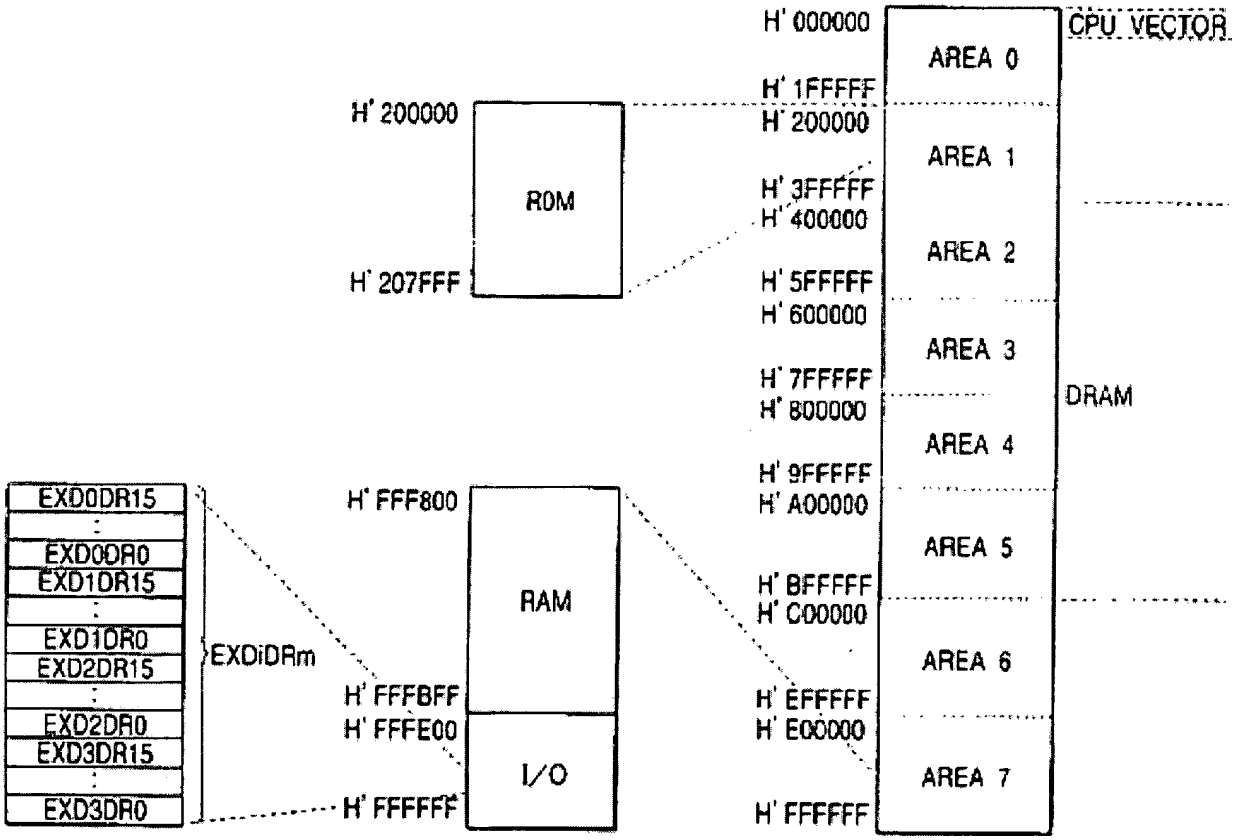
Independent claims 1 and 12 both recite an interface and first and second address maps, where the first address map allocates a first range of addresses an on-chip resource and a second range of addresses to the interface while the second address map allocates the first range of addresses to the interface. That is, the first range of addresses map to an on-chip resource in the *first address map* while that same first range of addresses map to the interface in the *second address map*; the second range of addresses map to the interface in the *first address map*. By way of further example, the specification describes a platform mode in which the address space includes a first portion allocated to memory resources 16, 18, etc. and a second portion allocated to the SHOC interface 20, as well as a bond-out mode in which the entire address space – including the first portion as well as the second portion – is allocated to the SHOC interface 20. Specification, pages 5–6. According to the specification:

> This allows two prototyping modes to be used depending on the nature of the system being developed, while utilizing the same evaluation chip 2. Platform mode allows a customer to preserve the address map of the evaluation chip 1, and integrate their IP only into the memory space occupied by the SHOC port while bond-out mode allows the user to decide to use the evaluation chip 2 only as a CPU core, using the entire memory space for their own IP.

Specification, page 6.

Such a feature is not found in the cited reference. First, contrary to the assertion in the Office Action, Figure 2 of *Mitsuishi* does NOT show two different address maps as asserted in the Office Action. Instead, Figure 2 illustrates only a single address map for the addresses within the range H' 000000 through H' FFFFFF that have been logically divided into a number of areas AREA 0 through AREA 7, with the addresses ranges allocated to ROM, RAM and I/O depicted together with the specific addresses within the I/O range that are allocated to particular data-transfer channel buffer registers:

FIG. 2



Mitsuishi, Figure 2. Only a single mapping of the address range H' 000000 through H' FFFFFF is depicted in Figure 2, not two different mappings for those addresses.

Second, *Mitsuishi* does not disclose allocating one range of addresses to an *interface* in a first mode and allocating another range of addresses to that same *interface* in a second mode. The cited portion of *Mitsuishi* merely teaches allocating different addresses ranges to a *memory* (ROM 5) in different modes:

> The ROM 5 has a typical size of 32 kbyte which is mapped onto addresses H' 200000 to H' 207FFF.

. . . .

> By setting a proper operating mode, the address range allocated to the embedded ROM 5 can be changed to area 0 . . .

Mitsuishi, column 14, lines 7–8 and column 15, lines 20–21. That is, .either a first address range (H' 000000 through H' 007FFF within AREA 0) or a second address range (H' 200000 through H' 207FFF within AREA 1) is allocated to ROM 5 depending on operating mode, but *Mitsuishi* does not teach that first and second address ranges are allocated to the I/O ports in different modes

Finally, *Mitsuishi* does not teach or suggest a single address range that is mapped to an on-chip resource in one mode and to an interface in a second mode. Instead, as noted above, *Mitsuishi* merely teaches that different address ranges – either a first address range (H' 000000 through H' 007FFF within AREA 0) or a second address range (H' 200000 through H' 207FFF within AREA 1) *in the same address map* – can be allocated to ROM 5 to allow for use of a processor (CPU) without an external ROM. *Mitsuishi*, column 14, lines 7–8 and column 15, lines 20–21. *Mitsuishi* does not teach that either of the two address ranges can be allocated first to ROM 5 in one mode and then to input/output (I/O) ports 21–26, 31–35 in a second mode.

Therefore, the rejection of claims 1–6, 8–9, 12–17 and 20–26 under 35 U.S.C. § 102 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckbutrus.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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